cofc

Attorney Docket No. 5649-1145 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Lee
Application Serial No.: 10/640,082
Filed: August 13, 2003
For: *Methods of Programming Non-Volatile Semiconductor Memory Devices Including Coupling Voltages and Related Devices*

U.S. Patent No.: 6,987,694
Issued: January 17, 2006

Date: May 4, 2006

Commissioner for Patents
Attn: Certificate of Correction Branch
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR ENTRY OF CERTIFICATE OF CORRECTION UNDER 35 U.S.C §254 AND 37 C.F.R. §1.322

Sir:

The Assignee of record for the above-referenced patent hereby requests, pursuant to 35 U.S.C §254 and 37 C.F.R. §1.322, that a Certificate of Correction be issued. This request is made in order to correct the mistakes incurred through the fault of the U.S. Patent and Trademark Office. No fee is believed due. However, the Commissioner is authorized to charge any deficiency or credit any overpayment to Deposit Account No. 50-0220.

The mistakes appearing in the patent are set forth with corrections on the Certificate of Correction enclosed herewith, with an additional copy thereof and a return post card.

Respectfully submitted,

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Certificate of Mailing under 37 CFR 1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, Attn: Certificate of Correction Branch, P.O. Box 1450, Alexandria, VA 22313-1450 on May 4, 2006.

Evelyn B. Casey

PTO/SB/44 (04-04)
Approved for use through 04/30/2007. OMB 0651-0033
Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,987,694

DATED : January 17, 2006

INVENTOR(S) : Lee

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 14,
Lines 24-25 should read -- second word line, applying a program voltage to a third word line connected to a third memory cell transistor of the string,

Line 27 should read -- sive to applying the program voltage to the third word line --

Line 29 should read -- the first and third memory cell transistors of the serially --

Column 15,
Line 13 should read -- nel of the third memory cell transistor with a first precharge --

Line 17 should read -- connected to the third word line with a second voltage --

Column 16,
Lines 57-58 should read -- a program voltage to a third word line connected to a third memory cell transistor of the string while applying the --

Lines 61-62 should read -- the third memory cell transistor being programmed responsive to applying the program voltage to the third word line --

Line 64 should read -- the first and third memory cell transistors of the serially --

Column 17,
Line 36 should read -- of the third memory cell transistor with a first precharge --

Line 40 should read -- connected to the third word line with a second voltage --

Column 18,
Line 6 should read -- supplying a program voltage to a third word line connected to --

Line 8 should read -- the first word line is closely adjacent to the third word line --

Line 27 should read -- each of the memory cell transistors stores 1-bit data. --

Line 48 should read -- lines being closely adjacent to a third word line connected to --

Column 19,
Line 16 should read -- being closely adjacent to a third word line connected to the --

Line 18 should read -- supplying a program voltage to the third word line , wherein the --

Line 55 should read -- first word line, a decoupling voltage to a third word line --

Column 20,
Line 14 should read -- **78**. The memory device according to claim **80**, wherein --

MAY 1 2 2006

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PATENT NO. 6,987,694
No. of additional copies: _____

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This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you are required to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.